

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A digital receiver for receiving an input signal produced using discrete multitone modulation, said receiver comprising:

an analog/digital converter to which the input signal is supplied, and

a time-domain equalizer connected downstream from the analog/digital converter, the time-domain equalizer including a digital filter having fixed coefficients, wherein the fixed coefficients of the digital filter have values that can be represented by shift operations.

2. (Previously Presented) The digital receiver as claimed in claim 1, wherein the fixed coefficients of the digital filter have integer values.

3. (Canceled)

4. (Previously Presented) The digital receiver as claimed in claim 1, wherein the digital filter has a zero at 0 Hz.

5. (Previously Presented) The digital receiver as claimed in claim 1, wherein the digital filter is a high-pass filter.

6. (Previously Presented) The digital receiver as claimed in claim 1, wherein the digital filter comprises a series of circuits, each of the circuits having a plurality of first-order digital filters.

7. (Previously Presented) The digital receiver as claimed in claim 6, wherein each first-order digital filter comprises:

Applicant : Heinrich Schenk  
Serial No. : 09/806,140  
Filed : March 27, 2001  
Page : 3 of 5

Attorney's Docket No.: 12816-008001 / S0751 SB/fis

a state memory,  
a shift register,  
a subtraction circuit, and  
an addition circuit.